



Design and Post-Layout Characterization of a CMOS Inverter in SKY130 Technology

Kunda Ganesh¹, Gannera Mamatha²

¹Department of Electronics and Communication Engineering, Jawaharlal Nehru Technological University College of Engineering, Anantapur, Andhra Pradesh, India.

kundaganesh502@gmail.com

²Associate Professor, Department of Electronics and Communication Engineering, Jawaharlal Nehru Technological University College of Engineering, Anantapur, Andhra Pradesh, India.

gmamatha.ece@jntua.ac.in

Abstract— *This work investigates the implementation and performance evaluation of a CMOS inverter standard cell in the SkyWater 130 nm open-source process design kit (SKY130). The circuit is developed and simulated using open-source electronic design automation tools, including MAGIC and NGSPICE.*

Important electrical characteristics such as transistor dimensions, switching behaviour, threshold voltage, noise margins, propagation delay, and signal transition times are evaluated to assess the inverter's performance. The physical layout is subsequently validated through design rule checking (DRC), layout versus schematic (LVS) verification, and parasitic extraction (PEX). The study demonstrates the feasibility of an open-source design and verification flow for CMOS standard-cell development, providing a cost-effective platform for VLSI and ASIC design research and experimentation.

Keywords— Custom Logic Gate Library, SkyWater 130nm PDK, SPICE Netlist, Liberty (.lib) File, Open-Source VLSI.

I. INTRODUCTION

Standard cell libraries serve as the fundamental building blocks of modern digital VLSI design [12]. By providing pre-designed, pre-verified logic primitives— such as inverters, NAND gates, NOR gates, and flip-flops— these libraries allow designers to focus on architecture rather than device level

implementation, dramatically accelerating the path from specification to silicon.

Historically, developing standard cell libraries demanded expensive proprietary tools and restricted Process Design Kits (PDKs), placing the work beyond the reach of most academic institutions and independent researchers. This changed with the 2020 release of the SkyWater 130nm open-source PDK (SKY130), developed through a collaboration between Google and SkyWater Technology [9]. SKY130 provides complete device models, design rules, and SPICE parameters for fabrication at the 130 nm node, at no cost, under an open-source license [1], [9].

Leveraging SKY130 and an entirely open-source EDA toolchain, this work presents the design and complete characterization of two CMOS inverter standard cells: INVX1 (minimum-width, single drive strength) and INVX2 (double drive strength). Both cells are developed through the full standard cell flow, from transistor sizing through Liberty file characterization, using MAGIC [11], NGSPICE [3], and Netgen [4]. The work produces a verified, characterized cell library entry with timing and power data directly usable in logic synthesis and static timing analysis (STA) tools [5].

II. RELATED WORK

Recent years have seen a growing body of research on open-source standard cell characterization using the SKY130 PDK. Rahman et al. [1] proposed a complete open-source characterization flow incorporating

MAGIC for layout, Netgen for LVS, NGSPICE for simulation, and Xschem for schematic capture, validating the approach on basic inverter cells. Their work established that the open-source flow produces results consistent with commercial EDA tools for simple cells, though they noted limitations when scaling to more complex logic.

Prior work has consistently employed MAGIC and NGSPICE as the primary design and simulation tools, with OpenROAD providing automated placement and routing [10]. Research has demonstrated that NLDM characterization using open-source tools matches commercial accuracy for the timing and power metrics required in Liberty file generation [14]. The present work builds upon this foundation by characterizing two inverter variants (INVX1 and INVX2), reporting both pre layout and post-layout timing, and providing a complete set of static and dynamic power data not commonly reported in prior studies

threshold close to $V_{DD}/2$, and minimum cell height of $2.72\mu\text{m}$ with abutment-compatible power rails.

B. Transistor Sizing

The PMOS transistor resides in the n-well (upper region) and the NMOS in the p-substrate (lower region), sharing a common polysilicon gate. For INVX1, the NMOS width is set to the PDK minimum $W_{n1} = 0.42\mu\text{m}$. Since electron mobility is approximately three times hole mobility ($\mu_n/\mu_p \approx 3$), the PMOS width required for symmetric rise and fall times is:

$$W_{p1} = \frac{\mu_n}{\mu_p} \times W_{n1} = 3 \times 0.42 = 1.26\mu\text{m} \quad (1)$$

For INVX2, double drive strength is achieved by doubling both transistor widths: $W_{n2} = 0.84\mu\text{m}$ and $W_{p2} = 2.52\mu\text{m}$ [17]. Channel length is $L = 0.15\mu\text{m}$ for both cells. The source/drain area and perimeter parameters for parasitic modeling are computed as:

$$A_s = A_d = W \times 2L_{min} \quad (2)$$

$$P_s = P_d = 2 \times (W + 2L_{min}) \quad (3)$$

where $L_{min} = 0.15\mu\text{m}$

III. METHODOLOGY

Fig. 1 illustrates the standard cell design flow followed in this work. Each stage is sequential and feeds into the next, ensuring that verification is performed at every step before committing to the subsequent phase.

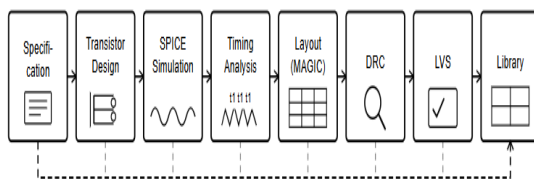


Fig. 1. Standard Cell Design Flow

A. Design Specifications

The technology node is SKY130 (130nm) [9], with a minimum channel length of $L = 0.15\mu\text{m}$. Supply voltage is $V_{DD} = 1.8\text{V}$ [18]. The design target is equal rise and fall times, a switching

TABLE I

TRANSISTOR SIZING PARAMETERS

Parameter	INVX1	INVX2
NMOS Width (W_n)	$0.42\mu\text{m}$	$0.84\mu\text{m}$
PMOS Width (W_p)	$1.26\mu\text{m}$	$2.52\mu\text{m}$
Channel Length (L)	$0.15\mu\text{m}$	$0.15\mu\text{m}$
Supply Voltage	1.8 V	1.8 V
Cell Height	$2.72\mu\text{m}$	$2.72\mu\text{m}$

C. SPICE Simulation Setup

The two inverters are connected in series (buffer configuration) as shown in Fig. 2. INVX1 is the cell under test; INVX2 serves as the load. The NGSPICE netlist [3] is fully parameterized with transistor widths and source/drain geometry expressions to enable rapid re-characterization under different sizing scenarios.

The stimulus is a rail-to-rail pulse from 0 to 1.8 V with 20 ps rise and fall times and a 2 ns period. Transient analysis runs for 10ns at a

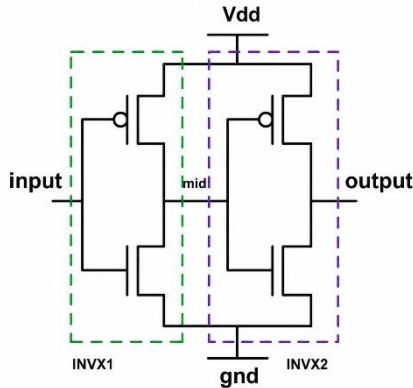


Fig. 2. IN VX1 driving IN VX2 as load (buffer configuration).

1ps time step. Measurements are: rise time t_r (20–80% of VDD), fall time t_f (80–20% of VDD), and propagation delay t_p (average of t_{pHL} and t_{pLH} at the 50% point).

D. Noise Margin

Noise margin defines the ability of a circuit to tolerate noise without affecting logic operation. It is derived from four VTC parameters: V_{IL} , V_{IH} , V_{OL} , and V_{OH} , where V_{IL} and V_{IH} are the unity-gain points ($dV_{out}/dV_{in} = -1$) on the VTC slope. The high-level and low-level noise margins are defined as:

$$NM_H = V_{OH} - V_{IH} \quad (4)$$

$$NM_L = V_{IL} - V_{OL} \quad (5)$$

Substituting the measured values:

$$NM_H = 1.746 - 1.006 = 0.740V \quad (6)$$

$$NM_L = 0.774 - 0.065 = 0.709V \quad (7)$$

Both margins exceed 39% of VDD, confirming strong noise immunity.

TABLE II
INVX1 NOISE MARGIN PARAMETERS
(TT CORNER, VDD = 1.8V)

Parameter	Value	Meaning
V_{IL}	0.774 V	Maximum LOW input recognised safely
V_{IH}	1.006 V	Minimum HIGH input recognised safely
V_{OL}	0.065 V	Output LOW voltage
V_{OH}	1.746 V	Output HIGH voltage
V_M	0.893 V	Switching threshold
NM_H	0.740 V	High-level noise margin
NM_L	0.709 V	Low-level noise margin

E. Physical Layout

Layouts are created in MAGIC [11] using SKY130 technology rules [9]. Both cells observe the standard row height of $2.72\mu m$, with VDD and GND power rails at the cell top and bottom for row-based abutment. The PMOS transistors occupy the n-well region (upper half) and NMOS transistors the p-substrate (lower half), connected by a shared polysilicon C. INVX1 Layout and Physical Verification gate. Metal1 is used for output and power routing. Contacts and vias follow SKY130 enclosure rules [9].

F. Design Rule Check (DRC)

DRC verifies the layout against all SkyWater foundry manufacturing rules [9]– minimum wire widths, spacing, enclosure rules, and contact requirements. The layout achieved zero DRC violations (DRC=0), as confirmed in Fig. 5, meaning it is fully ready for fabrication.

G. Layout Versus Schematic (LVS)

LVS comparison was performed using Netgen [4], comparing the netlist extracted from the physical layout against the original schematic netlist. As shown in Fig. 6, the tool reported “Circuits match uniquely” with both circuits containing 2 devices and 4 nets–

confirming the layout is electrically equivalent to the schematic.

H. Parasitic Extraction and Post-Layout Simulation

A full parasitic extraction (PEX) is performed in MAGIC using ext2spice with cthresh0 and rthresh0 [11] to capture all interconnect capacitances and resistances [6]. The resulting PEX netlist is used to re-run the NGSPICE transient simulation, providing post-layout timing results that include the degradation introduced by layout parasitics.

IV. SIMULATION RESULTS– INVX1

A. Transient Waveforms

Fig. 3 shows the NGSPICE transient output for the INVX1 INVX2 buffer chain. The red trace (offset +6V for clarity) is the input; the blue trace (offset +3V) is the INVX1 output at the mid node; the yellow trace is the final INVX2 output at 0–1.8 V. Clean square-wave outputs with sharp, symmetric transitions confirm correct inverter operation.

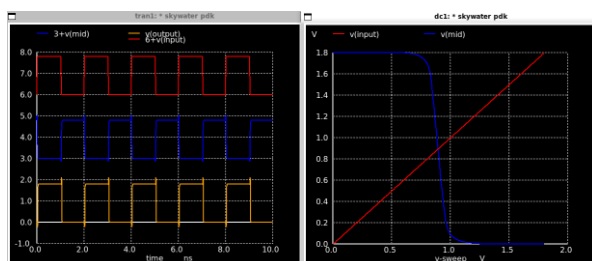


Fig. 3. Simulation results of INVX1: (a) Transient waveforms showing input (red), INVX1 output at mid node (blue), and INVX2 output (orange); (b) Voltage Transfer Characteristic (VTC)

B. Voltage Transfer Characteristics (VTC)

Fig. 3 shows the Voltage Transfer Characteristic (VTC) of INVX1 obtained by sweeping the input from 0V to 1.8V. The steep

S-shaped transition curve indicates high DC gain and strong noise immunity, with the switching threshold $V_M = 0.893V$ closely matching the ideal value of $V_{DD}/2 = 0.9V$. The output swings fully rail-to-rail from 0V to 1.8V, confirming correct inverter operation.

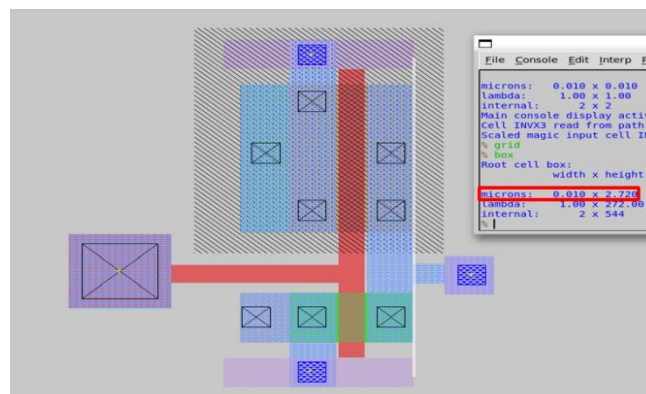


Fig. 4. INVX1 layout in MAGIC– cell height confirmed at 2.72 m.

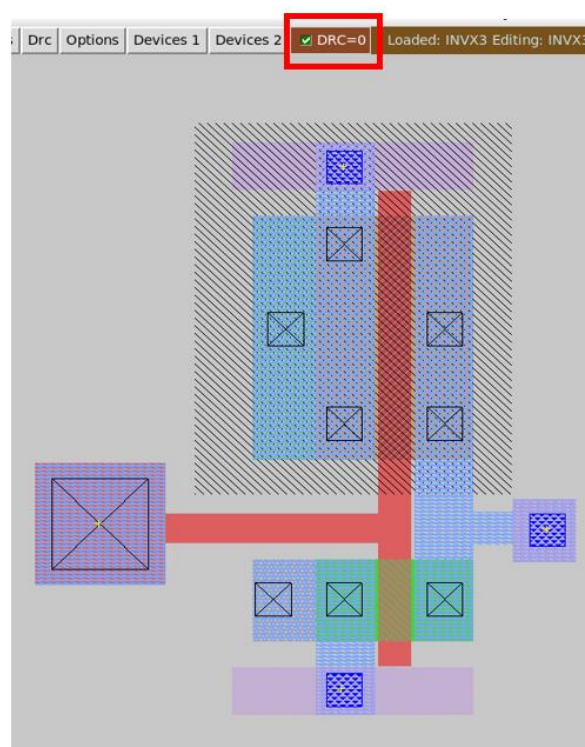


Fig. 5. INVX1 DRC result: DRC=0 (no violations). Layout is manufacturable.

C. INVX1 Layout and Physical Verification

Figs. 4 and 5 show the INVX1 physical layout in MAGIC with the cell height confirmed at $2.72\mu\text{m}$, and the DRC result showing zero violations. Fig. 6 shows the Netgen LVS output confirming both circuits (layout and schematic) contain 2 device instances and 4 nets, with the conclusion “Circuits match uniquely.”

```
Contents of circuit 1: Circuit: 'INVX1'
Circuit INVX1 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances: 1
  Class: sky130_fd_pr__pfet_01v8 instances: 1
Circuit contains 4 nets.
Contents of circuit 2: Circuit: 'INVX1'
Circuit INVX1 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances: 1
  Class: sky130_fd_pr__pfet_01v8 instances: 1
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets, Circuit 2 contains 4 nets.

Final result:
Circuits match uniquely.

Logging to file "comp.out" disabled
LVS Done.
```

Fig. 6. INVX1 LVS result (Netgen): circuits match uniquely — LVS Clean

D. INVX1 Dynamic Characteristics

TABLE III
INVX1 DYNAMIC CHARACTERISTICS

Parameter	Schematic	Post-Layout
Rise time (tr)	18.52 ps	20.55 ps
Fall time (tf)	18.51 ps	20.72 ps
Prop. delay (tp)	21.2 ps	23.16 ps

The rise and fall times of the near-identical schematic level (difference $< 0.01\text{ps}$) confirm that the 3:1 PMOS/NMOS sizing achieves the balanced-timing goal. Post-layout values show a 10–15% increase attributable to interconnect parasitics captured during PEX.

The propagation delay increased from 21.2ps to 23.16ps after parasitic extraction, indicating the effect of layout-induced resistance and capacitance. The small increase confirms that the physical layout closely matches the intended schematic behaviour. Nearly equal rise and fall

times demonstrate balanced PMOS and NMOS drive strengths achieved through the 3:1 sizing ratio. These results validate the INVX1 cell as a reliable and well-characterized standard cell for ASIC library development.

V. SIMULATION RESULTS– INVX2

INVX2 is designed with double drive strength ($Wn2 = 0.84\mu\text{m}$, $Wp2 = 2.52\mu\text{m}$). The wider transistors reduce on resistance, resulting in faster switching and lower propagation delay compared to INVX1. Figs. 7–9 show the INVX2 layout, DRC, and LVS results.

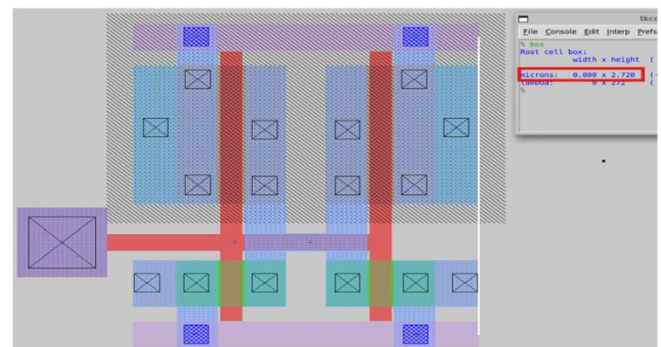


Fig. 7. INVX2 layout in MAGIC– cell height confirmed at $2.72\mu\text{m}$. Wider transistors are visible compared to INVX1

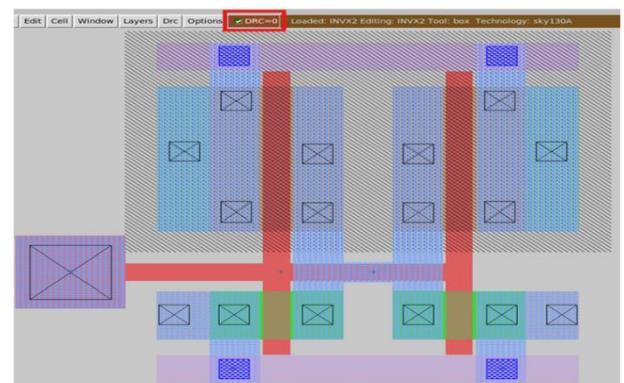


Fig. 8. INVX2 DRC result: DRC=0. Layout is manufacturable

INVX2 achieves approximately 36% lower propagation delay than INVX1 at the post-layout level (18.63ps vs. 23.16ps), consistent

with the expected behaviour of doubled drive strength. The slight asymmetry in post-layout rise and fall times (13.91ps vs. 14.00ps) is a consequence of layout dependent parasitic differences between the PMOS and NMOS diffusion regions. INVX2 achieves faster switching performance than INVX1 due to its increased transistor widths and higher drive strength. The reduced propagation delay and transition times demonstrate its suitability for driving larger loads in high-speed digital circuits.

```
Contents of circuit 1: Circuit: 'INVX2'
Circuit INVX2 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances: 1
  Class: sky130_fd_pr__pfet_01v8 instances: 1
Circuit contains 4 nets.
Contents of circuit 2: Circuit: 'INVX2'
Circuit INVX2 contains 2 device instances.
  Class: sky130_fd_pr__nfet_01v8 instances: 1
  Class: sky130_fd_pr__pfet_01v8 instances: 1
Circuit contains 4 nets.

Circuit 1 contains 2 devices, Circuit 2 contains 2 devices.
Circuit 1 contains 4 nets, Circuit 2 contains 4 nets.

Final result:
Circuits match uniquely.

Logging to file "comp.out" disabled
LVS Done.
```

Fig. 9. INVX2 LVS result (Netgen): circuits match uniquely– LVS Clean.

TABLE IV
INVX2 DYNAMIC CHARACTERISTICS

Parameter	Schematic	Post-Layout
Rise time (tr)	11.76 ps	13.91 ps
Fall time (tf)	11.15 ps	14.00 ps
Prop. delay (tp)	16.37 ps	18.63 ps

VI. INVERTER CELL CHARACTERIZATION

This section presents the mathematical formulas extracted from the SPICE netlists used to compute each characterization parameter. All simulations are performed using NGSPICE [3] with the Skywater130 TT corner models [18]. The input stimulus is a PULSE waveform from 0 to VDD (1.8V) with parameterized rise/fall slew times and output load capacitances.

A. Transition Time (Rise and Fall)

The output transition times are measured on the output node (mid) between the 20% and 80%

thresholds of VDD, as defined in the SPICE netlist.

$$trise = T(V_{out} = 0.8 \times VDD) - T(V_{out} = 0.2 \times VDD) \quad (8)$$

$$tfall = T(V_{out} = 0.8 \times VDD) - T(V_{out} = 0.2 \times VDD) \quad (9)$$

TABLE V

OUTPUT RISE TRANSITION TIME (NS) –
[INPUT SLEW VS OUTPUT CAPACITANCE]

Load \ Slew	10 ps	100 ps	1000 ps
0.5 fF	0.01164	0.02189	0.08951
10 fF	0.06761	0.06799	0.01829
100 fF	0.05978	0.05978	0.06100

TABLE VI

OUTPUT FALL TRANSITION TIME (NS) –
[INPUT SLEW VS OUTPUT CAPACITANCE]

Load \ Slew	10 ps	100 ps	1000 ps
0.5 fF	0.01202	0.01956	0.08014
10 fF	0.07207	0.07207	0.01741
100 fF	0.06410	0.06410	0.06476

where $T(x)$ denotes the simulation time at which the output voltage reaches threshold x . The SPICE .measure directive TRIG/TARG captures these time points automatically across a 3×3 sweep [14] of input slew (10ps, 100ps, 1000ps) and output load capacitance (0.5 fF, 10fF, 100fF).

B. Propagation Delay (Cell Rise and Cell Fall)

Propagation delay is measured from the 50% crossing of the input waveform to the 50% crossing of the output waveform [15], as specified in the netlist.

$$tp_{LH} = T(V_{out} = 0.5VDD, \uparrow) - T(V_{in} = 0.5VDD, \downarrow) \quad (10)$$

$$tp_{HL} = T(V_{out} = 0.5VDD, \downarrow) - T(V_{in} = 0.5VDD, \uparrow) \quad (11)$$

Here tp_{LH} corresponds to the cell rise delay (input falls, output rises for an inverter) and tp_{HL} corresponds to the cell fall delay (input rises, output falls). The TRIG condition is placed on V_{in}

and the TARG condition on Vmid, both at the 50% level ($0.5 \times V_{DD} = 0.9V$).

TABLE VII

CELL RISE DELAY (NS) – [INPUT SLEW VS OUTPUT CAPACITANCE]

Load \ Slew	10 ps	100 ps	1000 ps
0.5 fF	0.01370	0.03150	0.07654
10 fF	0.05263	0.07500	0.02176
100 fF	0.04144	0.04372	0.06670

TABLE VIII

CELL FALL DELAY (NS) – [INPUT SLEW VS OUTPUT CAPACITANCE]

Load \ Slew	10 ps	100 ps	1000 ps
0.5 fF	0.01759	0.03320	0.07209
10 fF	0.06463	0.08399	0.02135
100 fF	0.05003	0.05206	0.07263

C. Input Pin Capacitance

Input capacitance is extracted using a slow linear voltage ramp on the input, with the output clamped to prevent switching, as implemented in the SPICE netlist [11]. The capacitance is computed from the charge-current relationship:

$$C_{in} = \frac{-I_{avg}}{dv/dt} = \frac{-I_{avg}}{V_{DD}/T_{ramp}} \quad (12)$$

where Iavg is the average current drawn from the input voltage source, $V_{DD} = 1.8V$, and $T_{ramp} = 10ns$ is the total ramp duration. The negative sign accounts for the current direction convention in NGSPICE. The slope is:

$$\frac{dv}{dt} = \frac{V_{DD}}{T_{ramp}} = \frac{1.8}{10ns} = 1.8 \times 10^8 V/s \quad (13)$$

TABLE IX

INVERTER INPUT PIN CAPACITANCE

Input Pin	Rise Cap (pF)	Fall Cap (pF)	Avg Cap (pF)
A	0.00245544	0.00245544	0.00245544

The result confirms the capability of the generator to generate topology with different number of masters and slaves.

D. Static (Leakage) Power

Static power is measured at DC steady-state conditions by applying a fixed logic level (0 or 1) to the input and measuring the total supply current [7]. It is computed as:

$$P_{static} = V_{DD} \times I_{leakage} \quad (14)$$

TABLE X

INVERTER STATIC (LEAKAGE) POWER

Input Condition (A)	Power (nW)
0	40.43
1	71.07

where $I_{leakage}$ is the quiescent supply current when the input is held constant. For the inverter, this is measured at A=0 (PMOS OFF, NMOS conducting) and A=1 (PMOS conducting, NMOS OFF), yielding 40.43nW and 71.07nW respectively.

E. Dynamic Power (Rise and Fall)

Dynamic power is computed by integrating the instantaneous power waveform over a fixed time window centered on each switching event [14], as defined in the netlist. The instantaneous power is:

$$P_{inst}(t) = -V_{DD}(t) \times I_{VDD}(t) \quad (15)$$

The energy consumed during rise and fall transitions is obtained by integrating $P_{inst}(t)$ over a 2ns window centered on each switching event:

$$E_{rise} = \int_{4.5ns}^{6.5ns} P_{inst}(t) dt \quad (16)$$

$$E_{fall} = \int_{9.5ns}^{11.5ns} P_{inst}(t)dt \quad (17)$$

The average dynamic power during each transition is then:

$$P_{rise}(nW) = \frac{E_{rise}}{2ns} \times 10^9 \quad (18)$$

$$P_{fall}(nW) = \left| \frac{E_{fall}}{2ns} \right| \times 10^9 \quad (19)$$

The integration windows (4.5–6.5ns for rise, 9.5–11.5ns for fall) are aligned with the switching transitions of the PULSE stimulus (period = 10ns, pulse width = 5ns). The absolute value in (19) ensures a positive result, as the integrand can be negative depending on current direction convention [3].

TABLE XI

DYNAMIC RISE POWER (NW) – [INPUT SLEW VS OUTPUT CAPACITANCE]

Load \ Slew	10 ps	100 ps	1000 ps
0.5 fF	460690	443714	179398
10 fF	201381	199908	188456
100 fF	163598	161617	193009

TABLE XII

DYNAMIC FALL POWER (NW) – [INPUT SLEW VS OUTPUT CAPACITANCE]

Load \ Slew	10 ps	100 ps	1000 ps
0.5 fF	521456	890848	947517
10 fF	356651	576535	548750
100 fF	332898	370054	728237

VII. CONCLUSION

This paper presented the design and complete characterization of an inverter standard cell using the Skywater130 open source 130nm CMOS PDK [9]. The cell was designed with a 3:1 PMOS-to-NMOS width ratio [17] to achieve balanced switching, and

characterized using NGSPICE [3] across a 3×3 sweep of input slew and output load capacitance at the TT corner (VDD = 1.8V) [18].

The average input capacitance was measured as 0.002732pF, with rise and fall transition times of 0.01121ns and 0.01156ns at minimum load, confirming balanced timing. Propagation delays and dynamic power values follow expected NLDM behaviour across all slew and load conditions. Post-layout extraction (PEX) [11] showed a 10–15% increase over schematic values due to interconnect parasitics. The characterized data is suitable for Liberty format library generation [13] and integration into standard EDA flows [10]. Future work will extend this library to include NAND, NOR, XOR, and buffer cells with full multi-corner characterization [7]

VIII. FUTURE WORK

The current work will be extended to design and characterize a complete logic gate standard cell library including NAND, NOR, AND, OR, XOR, and buffer cells using the Skywater130 PDK. Multi-corner characterization (FF, SS, SF, FS) [7] will be performed to ensure robust timing closure across process variations. The generated Liberty (.lib) [13] files will be integrated into an open-source EDA flow using OpenROAD [10] for synthesis and static timing analysis (STA) [5].

REFERENCES

- 1) M. S. Rahman, Z. Kamal, S. H. Suvo, and T. Rahman, "Standard Cell Library Characterization Flow Using Open Source Tools with Google + SkyWater 130nm PDK," in Proc. 2024 6th Int. Conf. Electrical Engineering and Information & Communication Technology (ICEEICT), pp. 1175–1180, 2024, doi:



- 10.1109/ICEEICT62016.2024.10534506.
- 2) "Xschem schematic circuit editor," <https://xschem.sourceforge.io/stefan/index.html> (accessed Jan. 30, 2024).
 - 3) H. Vogt, "Ngspice, the Open Source Spice Circuit Simulator," <https://ngspice.sourceforge.io/> (accessed Jan. 29, 2024).
 - 4) "Netgen," Opencircuitdesign.com, 2019, <http://opencircuitdesign.com/netgen/>.
 - 5) "The-OpenROAD-Project/OpenSTA," GitHub, Jan. 24, 2024, <https://github.com/The-OpenROAD-Project/OpenSTA>.
 - 6) "The-OpenROAD-Project/OpenRCX," GitHub, Jan. 26, 2024, <https://github.com/The-OpenROAD-Project/OpenRCX>.
 - 7) A. P. Shah, V. Neema, and S. Daulatabad, "Effect of process, voltage and temperature (PVT) variations in LECTOR-B at 70nm technology node," in IC4, Indore, India, 2015, pp. 1–6, doi: 10.1109/IC4.2015.7375543.
 - 8) S. Nishizawa and T. Nakura, "Libretto: An Open Cell Timing Characterizer for Open Source VLSI Design," IEICE Trans. Fundamentals, vol. 106, no. 3, pp. 551–559, 2023.
 - 9) "google/skywater-pdk," GitHub, Jan. 30, 2024, <https://github.com/google/skywater-pdk>.
 - 10) M. Shalan and T. Edwards, "Building OpenLANE: A 130nm OpenROAD-based Tapeout-Proven Flow," in IEEE/ACM ICCAD, San Diego, CA, USA, 2020, pp. 1–6.
 - 11) "Magic Tutorial #8: Circuit Extraction," Magic VLSI Layout Tool, <http://opencircuitdesign.com/magic/tutorials/tut8.html>.
 - 12) "What is Library Characterization?" Synopsys, <https://www.synopsys.com/glossary/what-is-library-characterization.html>.
 - 13) T. VLSI, "LIB File in Physical Design," Team VLSI, May 2020, <https://teamvlsi.com/2020/05/lib-and-lef-file-in-asic-design.html>.
 - 14) "NLDM VS CCS," Physical Design for ASIC, <https://asicforphysicaldesign.blogspot.com/2015/01/nldm-vs-ccs.html>.
 - 15) "Transition on Delay Chip-VLSI and Design, Propagation Delay," ASIC-System <https://asic-soc.blogspot.com/2008/12/transition-delay-and-propagation-delay.html>.
 - 16) T. VLSI, "Library Exchange Format — LEF File," Team VLSI, May 2020, <https://teamvlsi.com/2020/05/lef-lef-file-in-asic-design.html>.
 - 17) "How delay of a standard cell changes with drive strength," VLSI Universe, 2017, <https://vlsiuniverse.blogspot.com/2017/12/how-delay-of-standard-cell-changes-with.html>.
 - 18) Efabless, "Skywater-PDK-libs-sky130 fd sc hd/timing," GitHub, [https://github.com/efabless/skywater-pdk-libs-sky130 fd sc hd/tree/master/timing](https://github.com/efabless/skywater-pdk-libs-sky130_fd_sc_hd/tree/master/timing).